Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] 1. A system for recovering the clock from an input data signal, comprising:

a rate detector for detecting a bit rate of the input data signal and providing a plurality of range signals specifying progressively high to low ranges encompassing said bit rate;

a frequency detector for providing a frequency error signal based on a difference in frequencies between the input data signal and a recovered clock signal;

a phase detector for providing a phase error signal based on the input data signal and said recovered clock signal;

a filter-controller for providing an oscillator driving signal based on said plurality of range signals, said frequency error signal, and said phase error signal; and

an oscillator-divider for providing said recovered clock signal based on said oscillator driving signal and at least some of said plurality of range signals;

and wherein:

said phase detector, said filter-controller, and said oscillator-divider collectively form a phase locked

loop.

[c2] 2. The system according to claim 1, wherein said rate detector includes a plurality of range sub-circuits each providing one of said plurality of range signals.

[c3] 3. The system according to claim 2, wherein said range sub-circuits include an input tailoring circuit for tailoring the input data signal, a filter for filtering the tailored input data signal, and an output tailoring circuit for tailoring the filtered input data signal into a respective said range signal.

[c4] 4. The system according to claim 1, wherein said phase detector further produces a recovered data signal based on the input data signal, thereby making the system suitable for use as a clock and data recovery circuit.

[c5] 5. The system according to claim 1, wherein said filter-controller includes:

an integrator for integrating said frequency error signal;

a plurality of amplifiers for amplifying the integrated said frequency error signal into a plurality of amplified said frequency error signals equaling said ranges in quantity; and

a switch for controllably selecting one amplified said

frequency error signal to contribute to said oscillator driving signal.

[c6] 6. The system according to claim 1, wherein said filter-controller includes:

a plurality of analog filters for filtering said phase error signal into a plurality of filtered said phase error signals equaling said ranges in quantity; and

a switch for controllably selecting one of said plurality of the filtered said phase error signals to contribute to said oscillator driving signal.

[c7] 7. The system according to claim 1, wherein said filter-controller includes:

a gated integrator for integrating said phase error signal;

a gated sample and hold circuit for sampling the integrated said phase error signal;

a frequency divider for dividing the frequency of said recovered clock signal, wherein the divided said recovered clock signal gates said gated integrator and said gated sample and hold circuit; and

a digital filter for filtering the sampled said phase error signal to contribute to said oscillator driving signal.

[c8] 8. The system according to claim 1, wherein said oscilla-

tor-divider includes:

a controllable oscillator producing an oscillating signal based on said oscillator driving signal; and

at least one frequency divider for dividing the frequency of said oscillating signal;

a switch for controllably selecting one from among said oscillating signal and the divided instances of said oscillating signal to contribute to said recovered clock signal.

[c9] 9. The system according to claim 8, wherein said controllable oscillator is a member of the set consisting of voltage controlled oscillators, current controlled oscillators, and digitally controlled oscillators.

[c10] 10. The clock and data recovery circuit according to claim 4 embodied in a receiver, wherein said receiver further comprises a photo diode for converting the input data signal from an optical form to an electrical form and providing it to the clock and data recovery circuit.

[c11] 11. The receiver according to claim 10, wherein said receiver further comprises conditioning circuitry for conditioning said electrical form of the input data signal prior to providing it to the clock and data recovery circuit.

[c12] 12. The receiver according to claim 11, wherein said sig-

nal conditioning circuitry includes a trans-impedance amplifier and a post amplifier.

[c13] 13. The receiver according to claim 10 embodied in a transceiver, wherein said transceiver further comprises a laser diode for converting said recovered data signal into an optical output data signal.

[c14] 14. The transceiver according to claim 13, wherein said transceiver further includes a frequency change circuit for converting said recovered data signal based on a clock other than said recovered clock signal.

[c15] 15. The transceiver according to claim 13, wherein said transceiver further includes a multiplexer for combining said recovered data signal and at least one other data signal into said optical output data signal.

[c16] 16. A method for recovering the clock from an input data signal, the method comprising the steps:

(a) detecting a bit rate of the input data signal and based thereon providing a plurality of range signals specifying progressively high to low ranges encompassing said bit rate;

(b) detecting a frequency error signal based on a difference in frequencies between the input data signal and a recovered clock signal;

(c) detecting a phase error signal based on the input data signal and said recovered clock signal;

(d) providing an oscillator driving signal based on said plurality of range signals, said frequency error signal, and said phase error signal; and

(e) providing said recovered clock signal based on said oscillator driving signal and at least some of said plurality of range signals, thereby using said phase error signal, said oscillator driving signal, and said recovered clock signal in the manner of a phase locked loop.

[c17] 17. The method according to claim 16, wherein said step (a) includes:

(1) tailoring the input data signal;

(2) filtering the tailored input data signal; and

(3) tailoring the filtered input data signal into a respective said range signal.

[c18] 18. The method according to claim 16, wherein said step (c) includes producing a recovered data signal based on the input data signal, thereby making the method suitable for use in both clock and data recovery.

[c19] 19. The method according to claim 16, wherein said step (d) includes:

(1) integrating said frequency error signal;

(2) amplifying the integrated said frequency error signal into a plurality of amplified said frequency error signals equaling said ranges in quantity; and

(3) controllably selecting one amplified said frequency error signal to contribute to said oscillator driving signal.

[c20] 20. The method according to claim 16, wherein said step (d) includes:

(1) filtering said phase error signal into a plurality of filtered said phase error signals equaling said ranges in quantity; and

(2) controllably selecting one of said plurality of the filtered said phase error signals to contribute to said oscillator driving signal.

[c21] 21. The method according to claim 16, wherein said step (d) includes:

(1) integrating said phase error signal;

(2) sampling the integrated said phase error signal;

(3) dividing the frequency of said recovered clock signal, wherein the divided said recovered clock signal gates said step (1) and said step (2); and

(4) filtering the sampled said phase error signal to contribute to said oscillator driving signal.

[c22] 22. The method according to claim 16, wherein said step

(3) includes:

(1) producing an oscillating signal based on said oscillator driving signal;

(2) dividing the frequency of said oscillating signal at least once; and

(3) controllably selecting one from among said oscillating signal and the divided instances of said oscillating signal to contribute to said recovered clock signal.

[c23] 23. The method according to claim 18, further comprising converting the input data signal from an optical form to an electrical form before further using it.

[c24] 24. The method according to claim 23, further comprising conditioning said electrical form of the input data signal before further using it.

[c25] 25. The method according to claim 23, further comprising converting said recovered data signal into an optical output data signal.

[c26] 26. The method according to claim 25, further comprising converting the frequency of said recovered data signal based on a clock other than said recovered clock signal.

[c27] 27. The method according to claim 25, further compris-

ing multiplexing said recovered data signal and at least one other data signal into said optical output data signal.